REMARKS:

This paper is herewith filed in response to the Examiner's Office Action mailed on January 4, 2007 for the above-captioned U.S. Patent Application. This office action is a rejection of claims 1, 3-15 and 17-23 of the application.

More specifically, the Examiner has rejected claim 22 under 35 USC 101 because the claimed invention is directed to non-statutory subject matter, rejected claims 1, 3-15, 17-21 and 23 under 35 USC 102(b) as anticipated by Saka (EP 0 689 324 A2). The Applicant respectfully addresses the rejections.

Claims 1, 21, 22 and 23 have been amended for clarification. Claims 1-15 and 17-23 have been amended for appearance. Claim 24 has been added. Support for these amendments may be found at least in paragraph 34 and paragraph 35 of the published US patent application (US 2002/0106992). No new matter is added.

Regarding the rejection of claim 22 under 35 USC 101, Claim 22 has been amended as suggested by the Examiner. The rejection of claim 22 under 35 USC 101 is now seen as overcome and the rejection should be removed.

Regarding the rejection of claims 1, 3-15, 17-21 and 23 under 35 USC 102(b). The Applicant respectfully traverses the rejection.

Claim 1 recites:

> An apparatus, comprising: a receiver for receiving a signal; and a synchroniser including a digital signal processor for processing the signal, wherein said synchroniser is configured to: provide a digital control signal, said control signal defining a plurality of different levels; control the level provided by successive ones of said control signals, successive ones of said control signal defining different values; convert said digital control signal into an analog control signal

> for controlling a mixing frequency; and estimate the difference between the levels of successive ones of said analog control signal, wherein said differences are used to estimate a step size between the successive analog control signal levels.

In the Office Action the Examiner states the following:

> Saka discloses a synchroniser for use in a receiver which receives signals, said synchroniser including a digital signal processor, said synchronizer configured to provide a digital control signal, said control signal defining a plurality of different levels; control the level provided by successive ones of said control signals, successive ones of said control signal defining different values; convert said digital control signal into an analog control signal for controlling a mixing frequency and estimate the difference between the levels of successive ones of said analog control signal. Saka further discloses a method of error correction as claimed (col. 24, line 1-col. 26, line 49; figure 4).

The Applicant notes that the rejection as stated is unclear. The Examiner broadly cites "col. 24, line 1-col. 26, line 49; figure 4," in the rejection of all the claims under 35 USC 102(b). However, no rationale is given by the Examiner to the Applicant to support the alleged anticipation of the individual claims of the present invention by the reference Saka. The Applicant respectfully requests clarification or removal of the rejection.

The reference cited by the Examiner discloses:

> "The frequency error detector 21 detects a frequency difference between the center frequency of the IF signal and the oscillation frequency of the VCO 25 based on the phase error signal sent from a phase detector 12," and "The frequency error is smoothed by the AFC loop filter 22 and sent to a D/A converter 24 via the latch circuit 23 and an adder 19 to be converted into an analog signal," and further "The resultant analog signal is input to the VCO 25 as a control signal," (col. 18, lines 29-37).

The Applicant contends that Saka does not "provide a digital control signal, said control signal defining a plurality of different levels," as claim 1 recites in part. As stated above, Saka discloses "The resultant analog signal is input to the VCO 25 as a control signal," (emphasis added). In addition, the Applicant further argues that Saka is not seen as anticipating that "said controlling and said estimating are performed in a digital domain," as in dependent claim 3.

Further Saka discloses:

> "When the detected frequency error is less than a reference value, an AFC hold signal is supplied to the latch circuit 23 from the frequency error detector 21. By the AFC hold signal, data for controlling the oscillation frequency of the VCO 25 is held by the latch circuit 23, and thus the VCO 25 operates at a constant oscillation frequency."

Thus, the Applicant contends that Saka is not seen to "control the level provided by successive ones of said control signals, successive ones of said control signal defining different values," as in claim 1.

The Applicant contends that Saka is primarily concerned with detecting frequency errors and is clearly distinguishable from the present invention for at least the reasons stated. Further, although the Applicant does not agree that Saka discloses or suggests the present invention, for mere clarification the independent claims 1, 21, 22, and 23 have been amended to further recite "wherein said differences are used to estimate a step size between the successive analog control signal levels."

Thus, in addition to the reasons already stated, the Applicant argues that Saka does not disclose or suggest "estimate[ing] the difference between the levels of the successive analog control signal, wherein said differences are used to estimate a step size between the successive analog control signal levels," as in the amended claim 1.

Furthermore, for at least the reason that the independent claims 21, 22, 23, and 24 recite language similar to that of claim 1 as noted above, Saka does not anticipate these claims, and all the independent claims 1, 21, 22, 23, and 24 should be allowed.

Moreover, as the claims 3-15 and 17-20 depend from claim 1, Saka does not anticipate these claims, and all the claims 1, 3-15, and 17-24 should be allowed.

Based on the above explanations and arguments, it is clear that Saka cannot be seen to anticipate claims 1, 3-15, and 17-24. The Examiner is respectfully requested to reconsider and remove the rejections of claims 1, 3-15, and 17-24 under 35 U.S.C. §102(b) and to allow all of the pending claims 1, 3-15, and 17-24 as now presented for examination. For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record. Should any unresolved issue remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted:

Harry F. Smith

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Date

Reg. No.: 32,493

Customer No.: 29683
HARRINGTON & SMITH, PC
4 Research Drive
Shelton, CT 06484-6212
Phone: (203) 925-9400
Facsimile: (203) 944-0245
Email: hsmith@hspatent.com

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